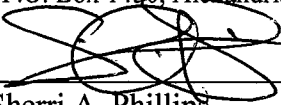


**RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE - EXAMINING GROUP 2100**

PATENT

I hereby certify that on the date specified below, this correspondence is being filed electronically via EFS-Web addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

March 30, 2009
Date


Sherri A. Phillips

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/822,275	Confirmation No. : 2177
Applicant : Jeffery W. Janzen	
Filed : April 8, 2004	Attorney Docket No.: 501286.01 (30262/US)
Art Unit : 2188	Customer No. : 27,076
Examiner : Shawn Eland	
Title : SYSTEM AND METHOD FOR OPTIMIZING INTERCONNECTIONS OF COMPONENTS IN A MULTICHIP MEMORY MODULE	

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 C.F.R. § 1.116

Sir:

Applicant acknowledges receipt of the Office Action dated February 12, 2009.
Any deficiency or overpayment of fees should be charged or credited to Deposit Account
No. 50-1266.

Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on
page 2 of this paper.

Remarks begin on page 9 of this paper.